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RECORD OF ORAL HEARING
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

EX PARTE SUNG-KYU CHOI

Appeal 2008-4828
Application 10/758,040
Technology Center 2100

Oral Hearing Held: February 11, 2009

Before JOHN C. MARTIN, JEAN R. HOMERE, and CAROLYN D. THOMAS, *Administrative Patent Judges*.

APPEARANCES:

ON BEHALF OF THE APPELLANT:

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1 The above-entitled matter came on for oral hearing on Wednesday,
2 February 11, 2009, at The U.S. Patent and Trademark Office, 600 Dulany
3 Street, Alexandria, Virginia, before Lorie B. Allen, Notary Public.

4
5 JUDGE MARTIN: You can proceed whenever you are ready.

6 MR. WALLERSON: Good morning again, Your Honors.

7 I'd first like to take a look at claim one. The basis of claim one --
8 there are four independent claims. I'd like to first focus on claim one.

9 The major contention that we have is that the two cited references,
10 Bourke and Barrenscheen, acknowledged by the Examiner, Bourke does not
11 disclose a multiplexer, the last element of the claim, wherein the multiplexer
12 receives first data from the processor and transfers the received first data, the
13 first memory, through a synchronous data bus, synchronized with the
14 processor, or receives second data from the first memory through a
15 synchronous data bus and transfers the second data to a processor.

16 The Examiner cites Barrenscheen as disclosing that cited limitation.
17 Apparently uses the bus interface B11 in Figure 4 as allegedly reading on the
18 claimed multiplexer.

19 Our position is that the bus interface cannot be construed as being a
20 multiplexer. There is no disclosure in the cited reference that that bus
21 interface could be used in any way as a multiplexer.

22 Further, we don't believe that bus one and bus two, which the
23 Examiner appears to assert, on the synchronous bus and asynchronous bus
24 could be construed as being synchronous and asynchronous buses. There is

1 no disclosure in the references that either one of those buses, either
2 synchronous or asynchronous --

3 JUDGE HOMERE: Counsel, let's go over your arguments one by
4 one. Let's start with the argument regarding the multiplexer. It calls for a
5 multiplexer that receives data and transfers data; right?

6 MR. WALLERSON: Correct.

7 JUDGE HOMERE: The Examiner's position is that the interface, the
8 bus interface, performs these same functions because it enables the data
9 transfer unit to receive data from one of the modules and then to transfer it to
10 another module.

11 Technically, would you agree this bus interface at least performs these
12 two functions, the function of receiving and transferring the data?

13 MR. WALLERSON: Maybe in terms of receiving one stream of data
14 and transferring that single stream, but there is no disclosure in the reference
15 that that bus interface may receive multiple streams and then multiplex that
16 into single streams of transfers to a bus.

17 JUDGE HOMERE: Does the claim require that the received data is
18 multiplexed before it is transferred? All you have is the nominal term of a
19 "multiplexer." Functions specific to the multiplexer being performed by the
20 multiplexer.

21 Really, for that matter, you could have any device that's capable of
22 transferring the data. You do agree that this bus interface performs the same
23 functions except you are alleging that for certain functions that are not
24 claimed, cited in the claim, are not being performed by the bus interface.

1 MR. WALLERSON: I would agree with that but also even if you
2 considered the bus interface to be a multiplexer, there is no disclosure in the
3 reference that that bus interface transfers data through a synchronous bus to
4 a first memory, and also there is no disclosure of asynchronous parts of the
5 claim.

6 JUDGE HOMERE: All right. You are conceding the argument
7 regarding the multiplexer. Now we are going to the
8 synchronous limitation--

9 MR. WALLERSON: Correct.

10 JUDGE HOMERE: How do you define "synchronous" and
11 "asynchronous?" What is the meaning of those terms?

12 MR. WALLERSON: "Synchronous" means -- well, as disclosed by
13 the specification, "synchronous" would mean that that bus is synchronized
14 with a processor clock-wise.

15 JUDGE HOMERE: Can you expand on that a bit more? What does
16 that mean, that the bus is synchronized with the processor?

17 MR. WALLERSON: The data on the synchronized bus is
18 programmed to send data based on certain clock signals, as opposed to the
19 asynchronous bus, where the data is stored in a buffer prior to being sent to
20 the asynchronous bus, so it's not really synchronized or sent in the same
21 time based on the processor.

22 JUDGE MARTIN: Is it fair to say that although the processor is
23 connected to the asynchronous bus and the synchronous bus, it only controls
24 the synchronous bus?

25 MR. WALLERSON: It only controls the synchronous bus.

1 JUDGE MARTIN: But it can still send information back and forth on
2 the asynchronous bus?

3 MR. WALLERSON: Through the buffer.

4 JUDGE MARTIN: The asynchronous bus, that's just not --

5 MR. WALLERSON: The data is first sent to a buffer as shown in
6 Figure 2 of the current invention. The data is sent to a buffer, to a
7 multiplexer, then to a buffer, and then sent to the second memory on the
8 asynchronous bus.

9 It is not synchronized with the processor as opposed to the
10 synchronized bus which is synchronized with the processor.

11 We don't see those limitations being shown in any of the cited
12 references, especially claim one, the Examiner uses Bourke and
13 Barrenschenn for those limitations.

14 JUDGE MARTIN: I wonder if you could tell me a little bit more
15 about our primary reference, Bourke. Doesn't the Examiner read the term
16 "multiplexer" on that interface 14 in Figure 2-A? He does call that a
17 "multiplexer," right?

18 I'm looking at the Answer, page three, halfway down, that last
19 paragraph, the line beginning "I.e., instruction processor, Unit 10A of Figure
20 1, is provided by a multiplexer," and then in parentheses "i.e. adapter
21 interface 14 of Figure 2-A."

22 I guess what I'm getting at is what's missing? Is it wrong to call that
23 a multiplexer or is it not functioning in the way that the claim requires the
24 multiplexer to function?

1 MR. WALLERSON: That's our point. We don't believe that even if
2 those are construed to be multiplexers, there is no disclosure. The crux of
3 the invention is sending data, to connect the processor to two different buses,
4 one synchronized and the other asynchronous, where with the asynchronous
5 transfer of data, it is sent to a multiplexer and then sent to a buffer prior to
6 being sent to the asynchronous bus.

7 I'm sorry. Correct, sent to a buffer prior to being sent to the
8 asynchronous bus.

9 There is no disclosure. Even if those elements may be construed to be
10 multiplexers, which we don't admit, there is no disclosure that data is being
11 sent to asynchronous buses or synchronous buses through a multiplexer,
12 through either of these elements.

13 JUDGE MARTIN: I'm sorry, counsel. I'm losing you on this
14 argument. In Figure 2-A, interface 14 is called by the Examiner a
15 multiplexer, and it has an adapter bus on one side that's synchronous, I
16 believe, it's described that way in the reference, and on the other side of this
17 interface, you have the SPD bus, which is described as asynchronous.

18 You have this multiplexer that's between an asynchronous bus and a
19 synchronous bus or you have this interface 14 anyway, that is between an
20 asynchronous bus and a synchronous bus. Is that correct?

21 MR. WALLERSON: We have two interface 14s.

22 JUDGE MARTIN: He called the whole thing 14. Okay. There are
23 three parts to that, aren't there. I don't know what you call that whole block.
24 He has called the upper adapter interface -- the reference refers to that as 14,
25 and the SPD bus interface is 12.

1 I see. The whole block is one of 10J, 10K, 10L, et cetera.

2 The Examiner, he was reading the claim, multiplexer, on just the
3 adapter interface 14, I guess.

4 JUDGE HOMERE: If you go to Figure 1, you have the SPD bus,
5 which is the synchronous bus. You have the IOICs, which is the
6 input/output interface controllers. The input/output interface controllers, this
7 is what the Examiner construed as being the multiplexer, and on the other
8 side, you have the adapter bus.

9 The input/output interface controller is better described in Figure 2
10 where it says it is comprised of a register and a variety of logic in there.

11 I guess the question that Judge Martin was asking was if the
12 input/output interface controller is the multiplexer and then you have the
13 asynchronous and synchronous buses, why would that not be -- how would
14 that be different from the current invention.

15 MR. WALLERSON: You still don't show any disclosure that the
16 data is being sent -- in terms of how the claim is drafted -- we have the
17 multiplexer that receives data from a first processor. That data is then sent
18 to a first memory through a synchronous bus.

19 The Examiner acknowledges that Bourke does not teach those parts,
20 those elements of the claim. Even if 14 is construed as being a multiplexer,
21 even the combination of Bourke and Barrenscheen do not disclose those
22 elements of a multiplexer receiving data from a processor, transferring that
23 data to a first memory through a synchronous bus.

24 JUDGE HOMERE: The argument here is we at least have come to a
25 preliminary agreement that the interface performed the function of the

1 multiplexer, so in Bourke, you have an asynchronous bus and a synchronous
2 bus, and then you have the interface that sits between them that enables one
3 to transfer data out from the synchronous bus or to the asynchronous bus.

4 Now, when you turn to Barrenscheen, this is the interface that enables
5 you to transfer data between a first module and a second module. I think
6 this is how the Examiner is trying to patch -- combine the references.

7 Technically, if you look at Figure 2 of Barrenscheen, you have the
8 first module that can be a computer or storage media, so you can send data --

9 MR. WALLERSON: I'm sorry. Figure 2?

10 JUDGE HOMERE: Figure 2-A of Barrenscheen.

11 If you send data from the first module over to that bus --

12 MR. WALLERSON: The first module being BU11?

13 JUDGE HOMERE: B11, this module can be a computer or a storage
14 media. Let's say it's a computer. You have a computer sending first data to
15 the interface, the interface receiving the data, transferring the data to the
16 second module via the bus, the first bus. That would read exactly on the
17 claim.

18 MR. WALLERSON: There is no disclosure that --

19 JUDGE HOMERE: The other thing that's missing here is the
20 synchronous limitation, that bus is synchronized to the computer.

21 MR. WALLERSON: Right; correct.

22 JUDGE HOMERE: If we go back to Bourke, because Bourke teaches
23 a synchronized bus and an asynchronized bus and having in between them
24 an interface.

1 I don't understand why the Examiner would not be able to rely on
2 Bourke for that limitation. In other words, having an interface that's capable
3 of transferring data to a synchronous bus. Unless you raise the argument
4 that the computer is not synchronized, the bus is not synchronized, the bus in
5 Bourke.

6 MR. WALLERSON: In Bourke; exactly.

7 JUDGE HOMERE: Don't let me put words in your mouth.

8 MR. WALLERSON: No. Right. That's an adapter bus. There is no
9 teaching that bus is synchronized with a processor.

10 JUDGE HOMERE: When you look at the disclosure of Bourke, it
11 says that the adapter bus is a synchronized bus, and the SPD bus is an
12 asynchronous bus. It's right there in column one and two.

13 You do have an interface that's interfacing, in other words,
14 transferring data between a synchronized bus and a computer.

15 MR. WALLERSON: There's no motivation to combine those
16 references in any case. There is no teaching in Barrenscheen that bus one or
17 bus two are synchronized or asynchronous in any way.

18 JUDGE HOMERE: There is synchronized teaching in Bourke.
19 Really, all you need Barrenscheen for is for the claimed structure. That is all
20 Barrenscheen provides you with is the ability to get data from a first
21 computer and transfer it over to a storage media via the interface, and vice
22 versa.

23 Really, the ability to send a first data and a second data over to the
24 other side via the interface and the bus.

1 Really, what is missing in Barrenscheen is the bus being synchronized
2 with the computer, the processor, but you have that teaching in Bourke.

3 Really, the bottom line is if it would have been much better to
4 combine these two here.

5 MR. WALLERSON: Our argument is one would not have been
6 motivated to combine those references.

7 JUDGE HOMERE: Why not?

8 MR. WALLERSON: We think the motivation would have to be in
9 the secondary reference, Barrenscheen.

10 JUDGE HOMERE: In the secondary reference? Why? Why could it
11 not be in the primary reference? What is the support, what is the legal
12 support for that?

13 You're familiar with KSR?

14 MR. WALLERSON: Yes.

15 JUDGE HOMERE: Someone who is not an attorney, someone who is
16 a competent person who is able to use common knowledge in order to come
17 up with a reasonable combination.

18 From putting these two references together -- I have the interface in
19 both references and then I have a synchronized bus and an asynchronous
20 bus, and I'm transferring data between a processor and a memory, therefore,
21 I have the invention.

22 MR. WALLERSON: In terms of the first and second memories, there
23 is no teaching that the data is being transferred -- well, even if you construe
24 the modules, there is no teaching that the data is being transferred to first and
25 second memories on those buses. I mean the modules --

1 JUDGE HOMERE: What do you mean? You have a bi-directional
2 transfer of data between the two modules.

3 MR. WALLERSON: You are construing the DTU, the data transfer
4 unit, as being the multiplexer.

5 JUDGE HOMERE: DTU; yes. The bus interface inside the data
6 transfer unit is the multiplexer, which is already provided in Bourke as the
7 input/output interface controller.

8 MR. WALLERSON: There is no teaching that interface has a
9 memory, a buffer, that can store the data prior to it being sent to a
10 synchronous bus.

11 JUDGE HOMERE: Yes, it does. Figure 2 of Bourke, the interface,
12 input/output interface controller 20, it has registers and buffers in it.

13 MR. WALLERSON: All right. The second rejection of claims two,
14 four and ten.

15 JUDGE MARTIN: Go right ahead.

16 MR. WALLERSON: A difference reference for claims two, four and
17 ten, Masayuki. We believe the same argument would also apply in this case
18 with regard to Masayuki.

19 We do not believe that Masayuki discloses the synchronized and
20 asynchronous buses. The Examiner cited Figure 3 and buses 33 and 34 as
21 allegedly reading on the synchronous and asynchronous buses, respectively.

22 There is no disclosure that bus 34 is synchronized or synchronous
23 with a processor. There is no disclosure that bus 33 is asynchronous.

24 JUDGE HOMERE: Let me read the Examiner's position regarding
25 Masayuki. The Examiner says that -- Figure 2 -- the Examiner says --

1 MR. WALLERSON: Figure 2 of Masayuki?

2 JUDGE HOMERE: Of Masayuki. The Examiner says the image data
3 bus, you are able to transfer data between the CCD sensor to the outside
4 memory unit, which is the image memory unit, item 32, via the
5 asynchronous bus.

6 The Examiner alleged that the image data bus is an asynchronous bus
7 and the CPU data bus is a synchronous bus.

8 MR. WALLERSON: We believe the Examiner is reciting subject
9 matter that is not taught or suggested by the claim, by the reference. There
10 is no teaching of those assertions in the reference.

11 JUDGE HOMERE: What do you think about -- when you look at
12 Figure 1, there is the sync generator that sends a signal to the image
13 generator unit, and then the image generator unit sends back synchronized
14 components. I'm referring to generator 26 that sends a signal.

15 Does this have anything to do with processor 20 being synchronized
16 with the image generator 10?

17 MR. WALLERSON: Correct.

18 JUDGE HOMERE: Do you see what I'm talking about?

19 MR. WALLERSON: Yes.

20 JUDGE HOMERE: 26 in Figure 20, a sync generator, sending a sync
21 signal to the image generator, which is 10. The image generator in return is
22 sending a signal back to the image processor, and that goes into the memory
23 controller 22 that distributes all the other signals to the other components in
24 the system.

1 MR. WALLERSON: I'm not sure how you're reading the
2 asynchronous aspect of that, by bus 33 being asynchronous, because they
3 seem to be connected -- those buses are connected together.

4 JUDGE HOMERE: Okay. You have a sent signal. The Examiner is
5 saying at least if you are assuming the sent signal that you're getting in there
6 goes through -- that's the same signal that's being fed to that bus, right, bus
7 33, that bus with respect to the image sensor would be de-synchronous.

8 MR. WALLERSON: They are both de-synchronous.

9 JUDGE HOMERE: The input, the CCD, I'm looking at Figure 2,
10 CCD and the image data bus, that would be synchronous to that bus.
11 However, when you look at CPU 41, that is connected to the CPU data bus,
12 the Examiner said that the way you communicate, that CPU communicates
13 with the image data bus is through three different interfaces.

14 MR. WALLERSON: We don't believe that. We believe they are
15 connected -- there is one connection between 33 and 34, between bus 33 and
16 bus 34.

17 JUDGE HOMERE: You have more than one connection. You have
18 that line, that direct line, 33 and 34. You have a JPEG Kodak 29 that
19 connects them together.

20 Really, the Examiner used the term "inherent."

21 MR. WALLERSON: Inherent; yes.

22 JUDGE HOMERE: The Examiner says those terms, "synchronous"
23 and "asynchronous" are not disclosed in this reference, but one of ordinary
24 skill in the art would know that, according to that configuration there.

1 MR. WALLERSON: That's the problem that we have. We don't
2 believe that inherency would actually work in this aspect, in this case. That
3 is reading subject matter into the reference that is distinctly not there.

4 JUDGE HOMERE: Okay.

5 JUDGE MARTIN: Do you have anything else?

6 MR. WALLERSON: No, sir.

7 JUDGE MARTIN: Thank you, counsel. We'll take the case under
8 advisement.

9 MR. WALLERSON: Thank you very much.

10 (Whereupon, the proceedings were concluded on February 11, 2009.)